DATA SHEET

UMA1021AM
Low-voltage frequency synthesizer for radio telephones

Product specification
Supersedes data of 1998 Mar 03
File under Integrated Circuits, IC17

1998 Nov 19

Philips Semiconductors

PHILIPS

Low-voltage frequency synthesizer for radio telephones

UMA1021AM

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021AM BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} for wider control range of the Voltage Controlled Oscillator (VCO), e.g. V_{DD} = 3 V and V_{CC} = 5 V.

The charge pump current (phase detector gain) is fixed by an external resistor at pin I_{SET} and controlled via the serial interface. Only a passive loop filter is necessary; the charge pump functions within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD}$	2.7	–	5.5	V
V_{CC}	analog supply voltage for charge pump	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{tot}	total supply current ($I_{DD} + I_{CC}$)	$V_{CC} = V_{DD} = 5.5$ V	–	10	–	mA
$I_{tot(pd)}$	total supply current in Power-down mode ($I_{DD} + I_{CC}$)	logic levels 0 V or V_{DD}	–	5	–	µA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference oscillator input frequency		3	–	35	MHz
$f_{ph(comp)}$	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

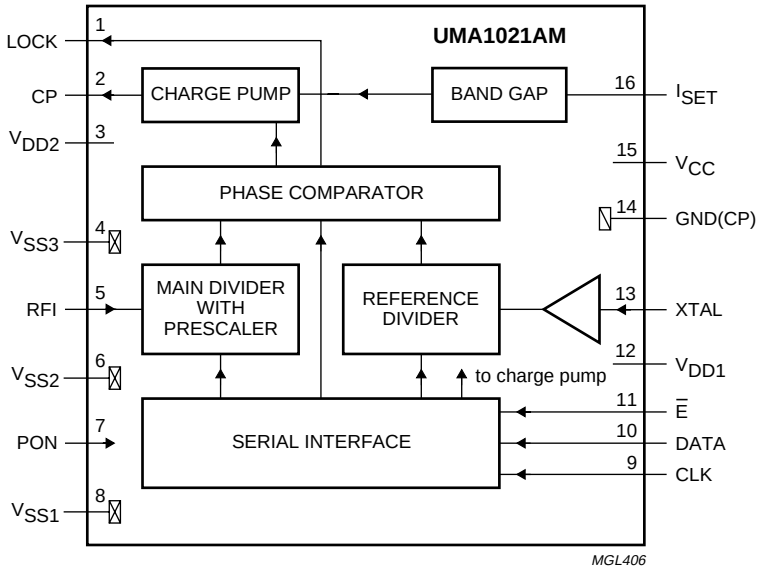


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	out-of-lock detector output
CP	2	charge pump output
V_{DD2}	3	digital supply voltage
V_{SS3}	4	ground 3 (0 V)
RFI	5	2 GHz main divider input
V_{SS2}	6	ground 2 (0 V)
PON	7	power-on input
V_{SS1}	8	ground 1 (0 V)
CLK	9	programming bus clock input
DATA	10	programming bus data input
$\overline{E}$	11	programming bus enable input (active LOW)
V_{DD1}	12	digital supply voltage
XTAL	13	crystal frequency input
GND(CP)	14	ground for charge pump
V_{CC}	15	analog supply voltage for charge pump
I_{SET}	16	charge pump current setting with external resistor from this pin to ground

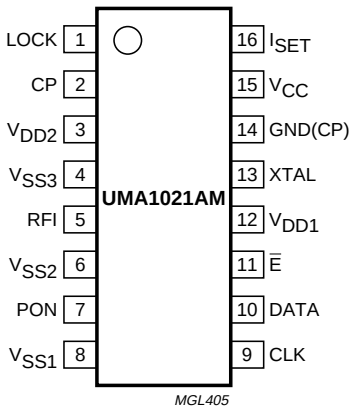


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main divider

The main divider is clocked at pin RFI by the RF signal which is AC-coupled from an external VCO. The divider operates with signal levels from 50 to 225 mV (RMS) and at frequencies from 300 MHz to 2.2 GHz. It consists of a fully programmable bipolar prescaler followed by a CMOS counter. The main divider allows programmable ratios from 512 to 131071 inclusive.

Reference divider

The reference divider is clocked by the signal at pin XTAL. The applied input signal should be AC-coupled. The circuit operates with levels from 50 up to 500 mV (RMS) and at frequencies from 3 to 35 MHz. Any divide ratios from 8 to 2047 inclusive can be programmed.

Phase comparator and charge pump

The phase detector is driven by the edges of the output signals of the main and reference dividers. The detector produces current pulses at pin CP. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, pin CP sinks current. If the reference divider edge arrives first, pin CP sources current.

The current at pin CP can be controlled via the serial programming bus as a multiple of the reference current set by an external pull-down resistor connected between pin I_{SET} and ground (see Table 2). Pin CP remains active except in the Power-down mode.

Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Out-of-lock detector

The out-of-lock detector is enabled or disabled via the serial interface by setting bit OOL (dt12) HIGH or LOW (see Table 1). An open-drain transistor drives the output pin LOCK. It is recommended to keep the sink current in the LOW state below 400 μA by applying a pull-up resistor from pin LOCK to the positive supply. When the out-of-lock detector is enabled pin LOCK is HIGH if the error at the phase detector input is less than approximately 25 ns, otherwise pin LOCK is LOW. If the out-of-lock detector is disabled, pin LOCK remains HIGH.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit.

The 3 lines are DATA (data bits), CLK (clock pulses) and $\overline{E}$ (enable signal). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the programming bus is inactive. It can always capture new programmed data even during power-down.

When the synthesizer is switched on, the presence of a signal at the reference divider input is required for correct programming.

Data format

The data format is shown in Table 1. The first bit entered is dt16, the last bit is ad0.

The leading bits (dt16 to dt0) make up the data field.

The four trailing bits (ad3 to ad0) are the address field. The UMA1021AM uses 4 of the 16 available addresses. These are chosen for compatibility with other Philips Semiconductors radio telephone ICs. The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

For the divider ratios, the first bits entered (PM16 and PR10) are the Most Significant Bits (MSBs).

The test register (address 0000) does not normally need to be programmed. However, if it is programmed all bits in the data field should be set to logic 0.

Power-down mode

The synthesizer is switched on when both the power-on input (PON) and the programmed bit dt6 (sPON) are HIGH. When switched on, the dividers and phase detector are synchronized to avoid random phase errors. When switched off, the phase detector is synchronized to avoid interrupting of the charge pump pulses.

The UMA1021AM has a very low current consumption in the Power-down mode.

Table 1 Bit allocation; note 1

FIRST IN										REGISTER BIT ALLOCATION										LAST IN
DATA FIELD																	ADDRESS			
dt16	**dt15**	**dt14**	**dt13**	**dt12**	**dt11**	**dt10**	**dt9**	**dt8**	**dt7**	**dt6**	**dt5**	**dt4**	**dt3**	**dt2**	**dt1**	**dt0**	**ad3**	**ad2**	**ad1**	**ad0**
test bits; note 2																	0	0	0	0
X	X	X	X	OOL[3]	X	CR1[4]	CR0	X	X	sPON[5]	X	X	X	X	X	X	0	0	0	1
PM16[6]	main divider coefficient															PM0	0	1	0	0
X	X	X	X	X	X	PR10[7]	reference divider coefficient									PR0	0	1	0	1

Notes

1. X = don't care.
2. The test register (address 0000) should not be programmed with any other values except all zeros for normal operation.
3. Bit OOL sets the Out-Of-Lock detector (1 = enabled).
4. Bits CR1 and CR0 set the charge pump current ratio (see Table 2).
5. Bit sPON sets the software power-up for the synthesizer (see Table 3).
6. PM16 is the MSB of the main divider coefficient.
7. PR10 is the MSB of the reference divider coefficient.

Table 2 Charge pump current ratio; note 1

BIT CR1	BIT CR0	CHARGE PUMP CURRENT
0	0	$10 \times I_{set}$
0	1	$18 \times I_{set}$
1	0	$13 \times I_{set}$
1	1	$17 \times I_{set}$

Note

1. Reference current for charge pump: $I_{set} = \frac{V_{set}}{R_{set}}$

Table 3 Power-on programming

PIN PON[1]	BIT sPON[2]	SYNTHESIZER STATE
L	X	off
X	0	off
H	1	on

Notes

1. Signal level
   a) L = LOW.
   b) X = don't care.
   c) H = HIGH.
2. X = don't care.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage		–0.3	+5.5	V
V_{CC}	analog supply voltage for charge pump		–0.3	+5.5	V
ΔV_{CC-DD}	supply voltage difference between the analog and digital supply voltages		–0.3	+5.5	V
V_n	voltage				
	at pins 5, 7, 9, 10 and 11		–0.3	V_{DD} + 0.3	V
	at pins 1, 2, 13 and 16		–0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between any of pins GND(CP), V_{SS1}, V_{SS2} and V_{SS3}	these pins should be connected together	–0.3	+0.3	V
P_{tot}	total power dissipation		–	85	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	operating ambient temperature		–30	+85	°C
$T_{j(max)}$	maximum junction temperature		–	150	°C

HANDLING

All pins withstand the ESD class 2 test in accordance with *“EIA/JESD22-A114-A”*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	142	K/W

CHARACTERISTICS

All values refer to the typical test and application diagram of Fig.5; $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins 3, 12 and 15						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD}$	2.7	–	5.5	V
V_{CC}	analog supply voltage for charge pump	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	total digital supply current of synthesizer ($I_{DD1} + I_{DD2}$)	V_{DD} = 5.5 V	–	7	9.5	mA
I_{CC}	analog supply current of charge pump	V_{CC} = 5.5 V; R_{set} = 5.6 kΩ	–	3	3.8	mA
$I_{tot(pd)}$	total supply current in Power-down mode ($I_{DD} + I_{CC}$)	logic levels 0 V or V_{DD}	–	5	50	µA
RF main divider input; pin 5						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	input signal level (RMS value)	AC-coupled; series resistance R_s = 50 Ω	50	–	225	mV
D/D_m	main divider ratio		512	–	131071	
Z_i	input impedance (real part)	f_{RF} = 1 GHz	–	750	–	Ω
		f_{RF} = 2 GHz	–	130	–	Ω
C_i	input capacitance	f_{RF} = 1 GHz	–	0.5	–	pF
		f_{RF} = 2 GHz	–	1.5	–	pF
Reference divider input; pin 13						
f_{xtal}	crystal reference oscillator input frequency		3	–	35	MHz
$V_{xtal(rms)}$	sinusoidal input signal level (RMS value)		50	–	500	mV
D/D_{ref}	reference divider ratio		8		2047	
Z_i	input impedance (real part)	f_{xtal} = 13 MHz	–	10	–	kΩ
C_i	input capacitance	f_{xtal} = 13 MHz	–	1.3	–	pF
Phase comparator						
$f_{ph(comp)}$	phase comparator frequency		–	200	–	kHz
$f_{loop(max)}$	maximum loop comparison frequency		–	2000	–	kHz
Charge pump current setting; pin 16						
R_{set}	external resistor	connected between pin 16 and ground	5.6	–	12	kΩ
V_{set}	regulated voltage	R_{set} = 5.6 kΩ	–	1.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump output; pin 2						
$V_{o(compl)}$	compliance output voltage	R_{set} = 5.6 kΩ	0.4	–	V_{CC} – 0.4	V
$I_{o(err)}$	output current error	R_{set} = 5.6 kΩ	–25	–	+25	%
$I_{o(match)}$	sink-to-source current matching	R_{set} = 5.6 kΩ	–	±5	–	%
I_L	leakage current	R_{set} = 5.6 kΩ; charge pump off; $V_{o(compl)} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
Phase noise						
N_{900}	RF synthesizer's contribution to close-in phase noise of 900 MHz VCO signal inside the closed loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; $f_{ph(comp)}$ = 200 kHz	–	–88	–	dBc/Hz
N_{1800}	RF synthesizer's contribution to close-in phase noise of 1.8 GHz VCO signal inside the closed loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; $f_{ph(comp)}$ = 200 kHz	–	–82	–	dBc/Hz
Interface logic inputs; pins 7, 9, 10 and 11						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
$I_{i(bias)}$	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_i	input capacitance		–	2	–	pF
Out-of-lock detector output; pin 1						
V_{OL}	LOW-level output voltage	open-drain output	–	–	$0.3V_{DD}$	V
$E_{\varphi(th)}$	threshold phase error	open-drain output	–	25	–	ns

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK						
t_r	rise time		–	10	40	ns
t_f	fall time		–	10	40	ns
T_{cy}	clock cycle time		100	–	–	ns
Enable programming; $\overline{E}$						
t_{START}	delay to rising clock edge		40	–	–	ns
t_{END}	delay from last falling clock edge		–20	–	–	ns
t_W	minimum inactive pulse width	note 1	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge		20	–	–	ns
Register serial input data; DATA						
$t_{SU;DAT}$	input data to clock set-up time		20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time		20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4000 ns when the both conditions are fulfilled:

   a) Main divider input frequency: $f_{RF} > \frac{447}{t_W}$

   b) Reference divider input frequency: $f_{xtal} > \frac{3}{t_W}$

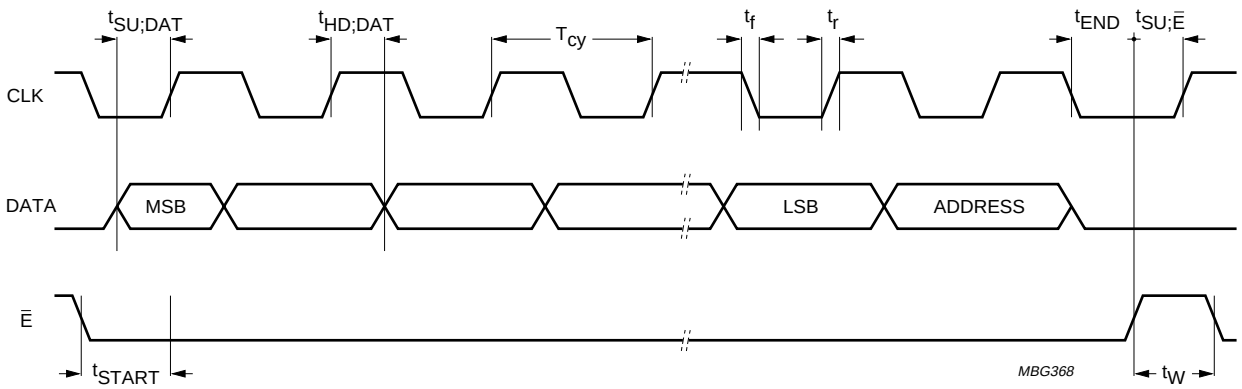


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

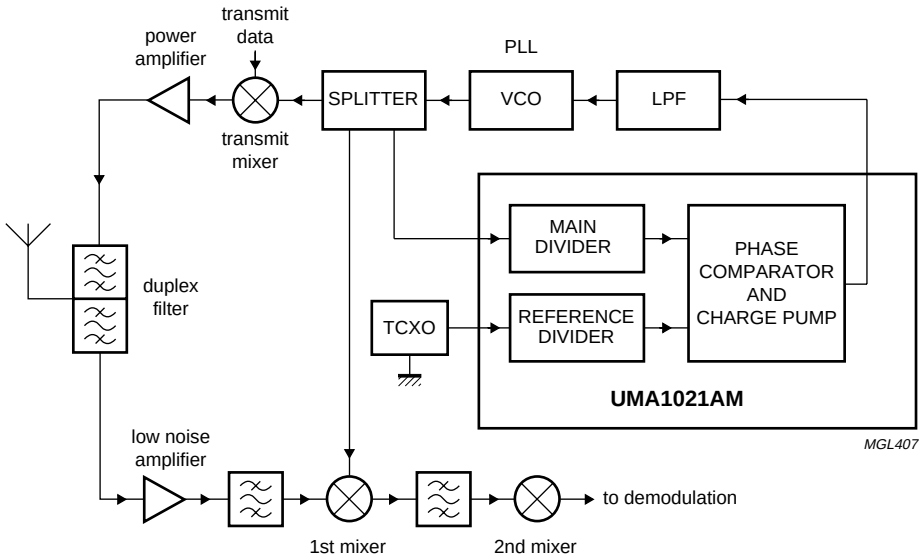
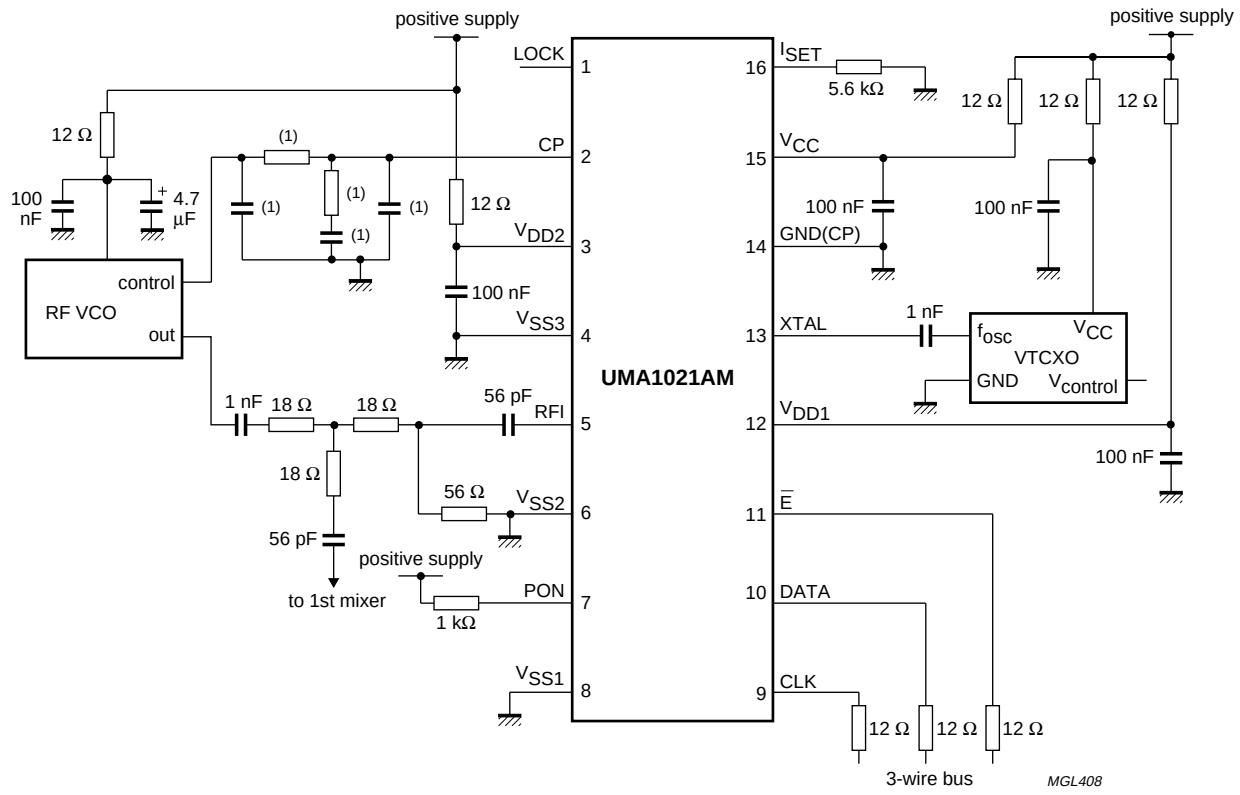


Fig.4 Typical application block diagram.

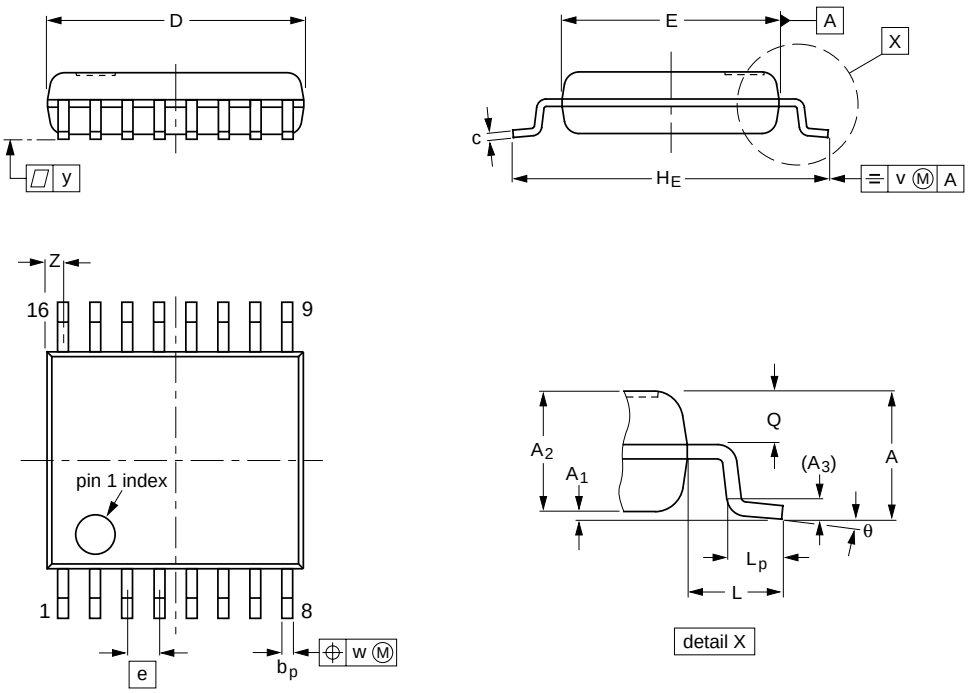


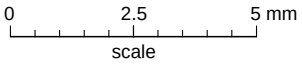
(1) Values depend on application.

Fig.5 Typical test and application diagram.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands 435102/750/02/pp16 Date of release: 1998 Nov 19 Document order number: 9397 750 04261

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